Q4 Known Good Substrates Technical Report
CONTRACT/PR NO. N00014-07-C-0918 Dow Corning Corporation
Quarterly Technical Report
Reporting Period: 1 June 2008 – 31 August 2008

Executive Summary

At the end of the fourth program quarter DCCSS has achieved step change improvements in crystal quality of 76mm diameter 4H n+ SiC crystals as assessed by MPD and HR-XRD. Crystals grown in this quarter now exhibit an MPD range of 1-5/cm^2. HR-XRD tests are showing significant reduction of mosaic structure. MPD and mosaic structure now reaching parity with long term suppliers of SiC wafers. In epitaxy, process improvements have reduced epitaxy defect density values to state of the art levels. Device data is now starting to emerge from subcontractors. Record breakdown strength and Vf values are achieved on PiN devices. Vf values are showing strong correlations to high carrier lifetime values measured on epilayers. Program is tracking to achieve most all metrics targets. Challenges remain on improving doping uniformity and reducing wafer resistivity.

Technical Progress

The following table documents the key program end metric goals.

Metric	50^{th} Percentile	20^{th} Percentile
MPD distribution 4H n+ 76 mm diameter (cm^{-2})	10	5
MPD distribution 4H n+ 100 mm diameter (cm^{-2})	20	10
Net scratch length by LLS relative to wafer diameter (%)	40	20
Equivalent Epitaxy Defect Density 76 mm diameter (cm^{-2})	<10	<5
Epitaxy Doping Target Accuracy	+/- 25%	+/-10%
Epitaxy Doping Variation within wafer (Max-Min/Min, %)	35%	10%
Substrate Resistivity Maximum 4H n+ 76mm	0.025	0.020

Progress against Metrics

The following charts show early progress against the program metrics. Due to extended processing cycles, data tends to become available 4-6 weeks in the rears.

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Loboda, Mark J.; Carlson, Eric P.; Chung, Gilyong; Lauer, Rebecca S.

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

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13. SUPPLEMENTARY NOTES

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The Known Good Substrates (KGS) Phase II program was initiated 29 August 2007. Wafer, epitaxy, modeling and metrology work has been the main focus of efforts in Q4. This technical report summarizes the progress by all team members against the tasks and milestones.

15. SUBJECT TERMS
SiC wafer, SiC epitaxy, SiC material metrology

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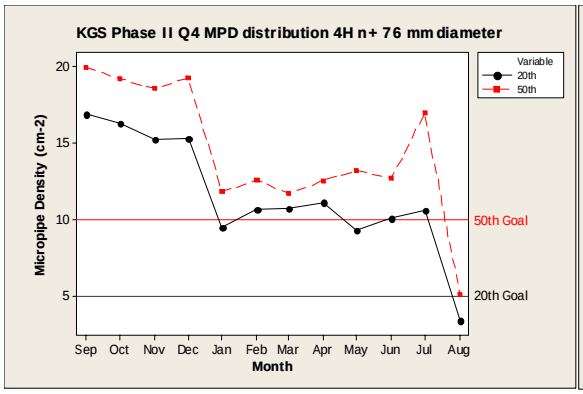
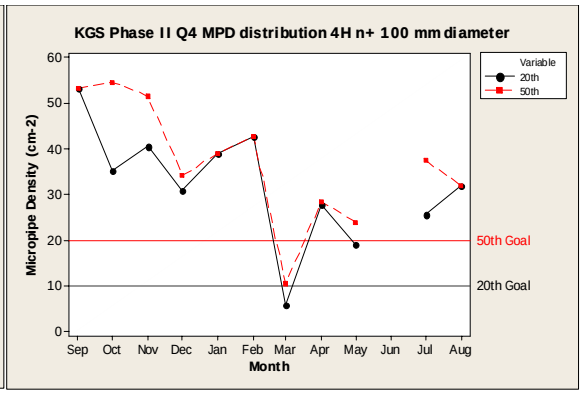
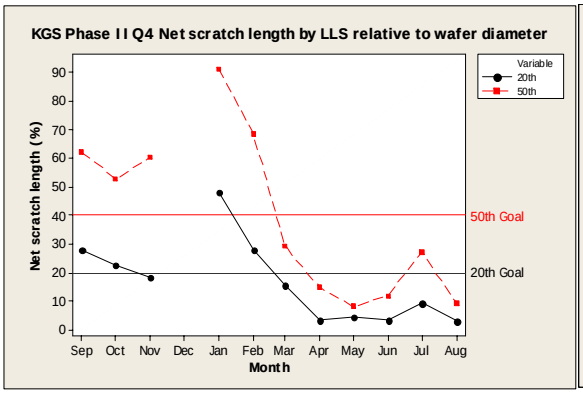
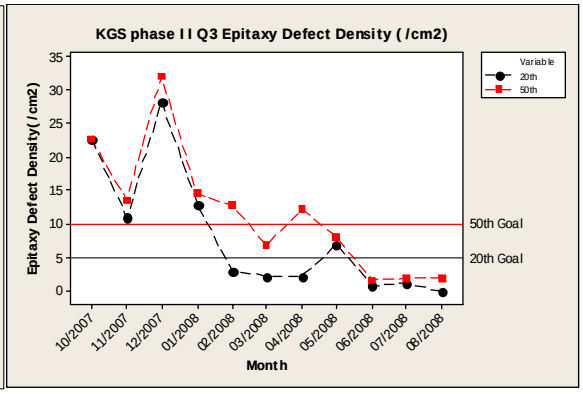
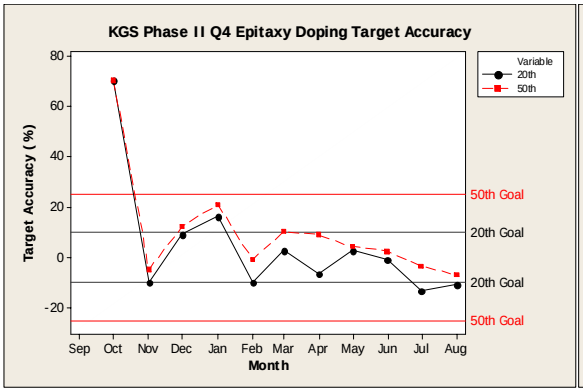
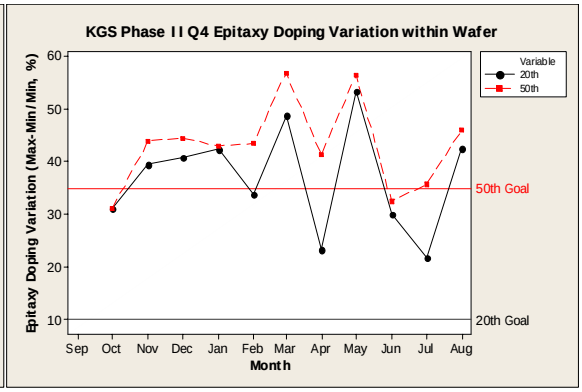

KGS Phase II Q4 MPD distribution 4H n+ 76 mm diameter
Micropipe Density (cm-2)
Month
Variable
20th
50th
50th Goal
20th Goal
Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug

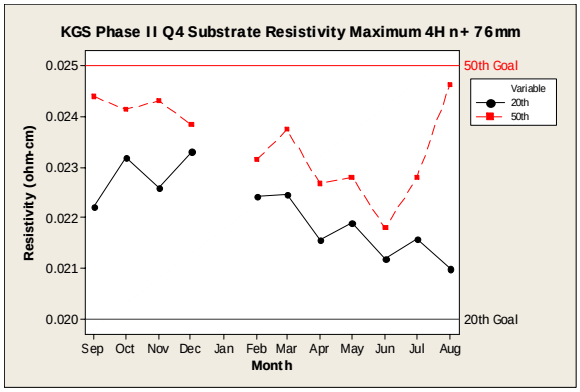

KGS Phase II Q4 MPD distribution 4H n+ 100 mm diameter
Micropipe Density (cm-2)
Month
Variable
20th
50th
50th Goal
20th Goal
Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug


KGS Phase II Q4 Net scratch length by LLS relative to wafer diameter
Net scratch length (%)
Month
Variable
20th
50th
50th Goal
20th Goal
Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug


KGS phase II Q3 Epitaxy Defect Density (/cm2)
Epitaxy Defect Density(/cm2)
Month
Variable
20th
50th
50th Goal
20th Goal
10/2007 11/2007 12/2007 01/2008 02/2008 03/2008 04/2008 05/2008 06/2008 07/2008 08/2008


KGS Phase II Q4 Epitaxy Doping Target Accuracy
Target Accuracy (%)
Month
Variable
20th
50th
50th Goal
20th Goal
20th Goal
50th Goal
Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug

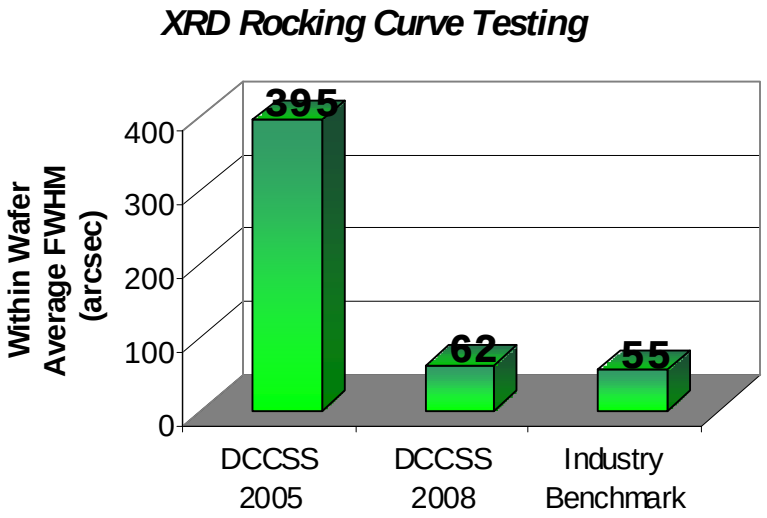

KGS Phase II Q4 Epitaxy Doping Variation within Wafer
Epitaxy Doping Variation (Max-Min/Min, %)
Month
Variable
20th
50th
50th Goal
20th Goal
Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug


KGS Phase II Q4 Substrate Resistivity Maximum 4H n+ 76mm
Resistivity (ohm-cm)
Month
Variable
20th
50th
50th Goal
20th Goal
Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug

Project Milestones
Task 1: SiC Wafers Products

Highlights:

- Transition to the next generation improved PVT growth process implemented in Q2 is complete and the new method is currently used for all PVT growths. The improved process has consistently maintained low micropipe densities for 76mm n+ 4H materials. The 20th percentile for Q4 is at 9.5 cm^{-2}, while the August 20th percentile is at 3.5 cm^{-2}. In addition to step change improvements in micropipes, the mosaic structure of the crystal is also reduced as evidenced by HR-XRD rocking curve measurements. The following bar chart shows the typical improvements in 4H n+ since 2005 when the first DCCSS 76mm wafers were produced.



- Defect analysis indicates that wafer polishing continues to meet the 50th and 20th percentile goals of the program for scratch defects.
- Improvements in the epitaxial growth process implemented in Q3 continue to produce material with low epitaxy defect density in Q4 of the program.
- All the epitaxial wafer deliverables have been completed and shipped to the program contract partners, including GeneSiC, MicroSemi, Northrop Grumman, NRL, and ASU, for device fabrication and testing.

Roadblocks:

- Failure analysis of cracking problems observed early in the transition to the new PVT process revealed that ingot grinding procedures could be adjusted to address the issue. Grinding yields have improved significantly in the last 8 weeks.
- Micropipe targets for 100mm still not at project goals. Transition to the new PVT growth process is now in progress. Due to the nature of the new process expansion work will be re-initiated in order to achieve 100mm 4H material that is

of comparable quality to the 76mm material. This will delay 100mm material availability for about 4 months.

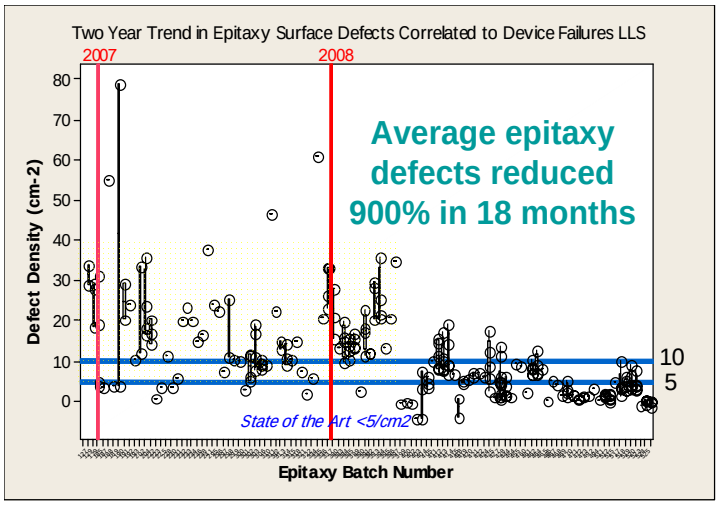
- Failure analysis efforts on polishing scratches indicate that variability of the lap slurry particle size is a likely source of deep scratches that impact final polish scratch length results. DCCSS is working with vendors to rectify the slurry abrasive particle size control.
- Epitaxial doping uniformity continues to be a challenge with uniformity values tracking higher than the 50^{th} percentile goal. Failure analysis shows that the primary doping variations occur in the last 10mm of the wafer. Epitaxy chemistry modeling efforts have highlighted that the current process, the spatial distribution of carbon containing species is unfavorable to get highly uniform doping to the wafer edge. Adjustments are being made to the reactor hardware and process conditions to improve the doping.

Project Milestones

Task 2: Continuous Improvements in SiC Substrates

Highlights

- Full implementation of the improved PVT growth process has resulted in an increased micropipe reduction rate with growth process optimization as seen by the large decrease in the last month of Q4. Through analysis of growth data for Q1 and Q2, DCCSS was able to adjust the crucible and source configurations, along with the growth nucleation conditions to be more favorable to eliminate stresses in the crystal and micropipes.
- Chemical-Mechanical Polishing trials and the results show surface roughness near 0.15 nm on a 20µm AFM scan and microscope inspections shows removal of fine scratches (visible at 200x or higher magnification). In Q5 wafers processed with CMP will be tested in epitaxy.
- Improvements in the epitaxial growth process implemented in Q3 continue to produce material with low epitaxy defect density (<2 cm^{-2}) in Q4 of the program. Modeling efforts showing distributions of reactants in the chamber shed light on process adjustments which led to a step change reduction in particle generation. This is the second step change improvement in 2008 as indicated by the chart below:



- The improved growth furnace RF heat source delivered in Q3 has been installed into a PVT furnace and is undergoing testing in Q4. Early results show improved polytype stability during growth conditions traditionally marginal in stability with the legacy heat source.

Roadblocks

- The improved PVT growth process has resulted in a larger variation for wafer resistivity as seen by the larger difference between the 20^{th} and 50^{th} percentile. However, the 20^{th} percentile target value was still not achieved. In order to meet target values for wafer resistivity, modification of the growth process will be required. Now that transition to the new PVT process is reaching a level of process consistency with respect to defect yields, resistivity tuning will be applied in Q5.

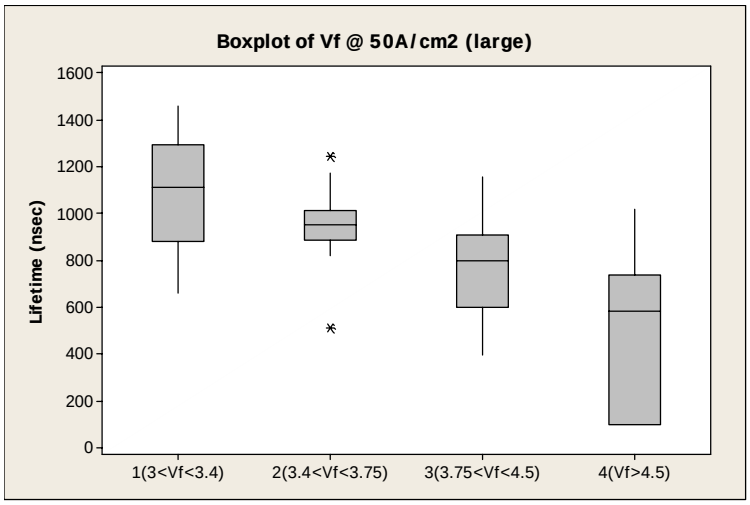
Task 3. Metrology for wafer specifications

Highlights

- LLS post epitaxy defect yield prediction methods have been compared with electrical probe data collected on PiN diodes. Difference between predicted and measured yield for PiN diodes is very comparable to that from SBD. LLS test can be used to get the full quality area test for the PiN diode application.
- Photoluminsescence (PL) imaging and optical stressing of a PiN wafer was conducted at ASU to monitor stacking fault (SF) propagation. Scanned laser-induced optical stress (SLIOS) system at room temperature was used. SF images with optical stressing are correlated with surface Nomarski images and no strong correlation has been observed between surface scratches and SFs.

Task 4. Device Technology Maturation

- MOS – Generation lifetime of SiC MOS capacitors shows big reduction with some process changes such as RIE and O_2 plasma etching on the epitaxy surface. Also defect decoration with point defects or metal impurities is suggested to explain large variation of generation lifetime in a small area. Therefore, generation lifetime can be used for epitaxy defect and oxide process control monitoring for SiC MOSFET. Preliminary data on MOS capacitors from 4 degree off epi-wafers is very promising to achieve low interface density and high threshold voltage for SiC MOSFET.
- PiN diode – 20um drift layer epitaxial wafers have been processed to make PiN diodes at GeneSiC. Both reverse and forward characteristics are evaluated on the wafer level tests. Blocking voltages above 3.4kV have been achieved on both 1mm and 0.5 mm devices. These correspond to 96% of the theoretical breakdown voltage of a 20 um epitaxial wafer. As far as we are aware, no previous result has achieved this high of an electric field in high voltage devices. Also on-state characteristics are equally impressive. On-state drops (at 100A/cm^2) less than 3.4V are demonstrated on 1 mm devices. On some 0.25 mm devices, we were able to get ~ 3.15V at 100A/cm^2, which is near-theoretical on-state drop for 4H-SiC PiN. Vf (@50A/cm^2) uniformity (sigma/mean) shows 5.5% on a 3" epi-wafer.
- Recombination lifetime vs. forward voltage drop (Vf) of PiN diodes – wafer level recombination lifetime testing has been employed at DCCSS. Vf of recent processed PiN diodes are correlated with carrier recombination lifetimes via electrical data maps and microwave PCD maps. It is clear that longer recombination lifetime in eptiaxy layer shows lower Vf of PiN diodes. This data supports that DCCSS can use recombination lifetime wafer maps to predict forward characteristics of PiN diodes.



Progress toward Milestones for End of Program (Sub-bullets are progress this quarter)

- Correlation Maps of PiN forward IV characteristics and recombination lifetime
  - Showing very good correlation between recombination lifetime and Vf of PiN
- Correlation of PiN forward IV characteristics and n+ epitaxial buffer layer/MP blocking
  - Thick n+ buffer wafers need special processes since the standard fab was not able to process them due to high density of stadium defects. Metal blanket and scoring approach have been selected. Four wafers with different buffer thicknesses are processed with this approach and testing is underway.
- Primary SiC material defect limiting PiN performance (Roadmap input - GeneSiC)
  - LLS can predict catastrophic reverse failures in PiN and recombination lifetime maps show correlations to Vf of PiN.
- SiC materials parameter assessed as most important for SIT performance improvements based on wafer probe data (Roadmap input - NGES)
  - First lots are now in device fabrication. No device data to report at this time.
- SiC materials parameter assessed as most important for SBD performance improvements based on wafer probe data (Roadmap input - Microsemi)
  - SBDs in testing at Microsemi. Preliminary SBD data was delivered to DCCSS in late August. Correlation analysis in progress.
- Generational improvement of 4H SiC wafer crystal quality summarized by XRT and MPD analysis
  - XRT discovered grain boundaries were nucleating in the crystal at the start of growth. By altering the nucleation growth parameters these grain boundaries new are no longer nucleated. XRT topography showed that scratches of the wafer surface lead to the nucleation of basal plane/threading dislocations loops, screw dislocations loops and ultimately carrot defects in epitaxy. It has also been used to show that scratches in seeds lead to the nucleation of threading screw dislocation loops, the building blocks for micropipes, in PVT crystals.
- Assessment of oxide quality for 76mm/100mm 4H epiwafers and link to generation lifetime
  - Wafers still in test at NRL and ASU.

<u>Schedule</u>

PiN diode fabrication work is near completion. SIT and SBD device fabrication work is still at 8 weeks behind schedule.

<u>Program Management</u>

Brian Russell accepted a new role within Dow Corning. Transition of program management responsibilities was transferred to Becky Lauer during this quarter.

Appendix 1: KGS Subcontractors and Quarterly Progress Points

Subcontractor	Area of Focus	Progress This Quarter
Northrup Grumman Electronics Systems	J-SIT fabrication and testing	Last set of epiwafers delivered in early August.
Microsemi	SBD fabrication and testing	SBD devices are fabricated and tested. Data on first lot delivered in August. First JTE design has a problem leading to arcing during testing; and the design and mask were adjusted. Lots 2,3 and 4 in progress.
GeneSiC Semiconductors	PiN diode fabrication and testing	All 17 epiwafers have been processed. Testing of forward and reverse I-V characteristics is near completion.
SUNY – Stoney Brook	Crystal Structure of SiC	XRT discovered grain-boundary nucleation at the start of growth and scratches in seeds leading to the nucleation of screw dislocation loops, the building blocks for MP.
Arizona State University	SiC Oxides, carrier lifetime and device failure analysis	PL imaging and optical stressing are conducted on PiN epiwafers. No strong correlation between surface scratches and SFs (Dr. Skromme) Genereation lifetime shows huge reduction with some process changes (e.g etching, O2 plasma). (Dr. Schroder)
Fluxtrol	Modeling and design of high uniformity induction heating systems	First successful growths of 4H SiC crystals using new heating systems were achieved in August. DOE now in progress to compare new and legacy heaters and the impact on SiC crystal

		growth.
NRL	SiC Oxides, Epitaxy, Lifetime testing, materials testing, device testing	All pre-fab characterization is done and PiN diode fab started.
STR	Modeling of CVD and PVT SiC Growth Processes	Focus this quarter on modeling CVD epitaxy. Results show impact of distribution of reactants on particle formation and uniformity. Now iterating epi model and epi experiments to improve doping uniformity.

Publications

ECSCRM 2008

1. Carrier Generation Lifetimes in 4H-SiC Epitaxial Wafers

Gil Chung**,** M.J. Loboda, M.J. Marninella, D.K. Schroder, T. Isaacs-Smith and J.R. Williams

2. Wafer Level Recombination carrier lifetime measurements of 4H-SiC PiN Epitaxial Wafers

Gil Chung**,** M.J. Loboda, M.F. MacMillan, and J.W. Wan

3. The Effect of 4H-SiC Substrate Surface Scratches on Chemical Vapor Deposition Grown Homo-Epitaxial Layer Quality

Ning Zhang, Yi Chen, Edward K. Sanchez, David R. Black and Michael Dudley